1. A transistor structure, comprising:

a gallium arsenide (GaAs) semiconductor substrate;

an indium aluminum arsenide (InAlGaAs) barrier layer disposed over the substrate;

an $In_y Ga_{1-y} As$ lower channel layer disposed on the barrier layer, where y is the mole fraction of In content in the lower channel layer;

an $In_x Ga_{1-x} As$ upper channel layer disposed on the lower channel layer, where x is the mole fraction of In content in the upper channel layer and where x is different from y; and

an InAlAs Schottky layer on the $In_x Ga_{1-x} As$ upper channel layer.

2. The transistor structure recited in claim 1 wherein the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

3. The transistor structure recited in claim 1 wherein the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

4. The transistor structure recited in claim 1 wherein x is in the range between 0.15 and 0.90 and y is in the range between 0.0 and 0.65.

5. The transistor structure recited in claim 4 wherein x is substantially 0.53 and y is substantially 0.43.

6. A transistor structure, comprising:

a semiconductor substrate;

an barrier layer disposed over the substrate;

a lower channel layer disposed on the barrier layer;

an upper channel layer disposed on the lower channel layer, such lower channel being of the same material as the upper channel, the upper and lower channels having different mole fractions of an common element used in such upper and lower channel layers; and

a Schottky layer on the upper channel layer.

7. The transistor structure recited in claim 6 wherein the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

8. The transistor structure recited in claim 6 wherein the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

9. The transistor structure recited in claim 7 wherein the substrate comprises GaAs and wherein the upper and lower channel layers comprise InGaAs.

10. The transistor structure recited in claim 9 wherein the upper and lower channel layers include indium.

11. A transistor structure, comprising:

a gallium arsenide (GaAs) semiconductor substrate;

a lattice matching structure disposed over the GaAs substrate, such layer comprising InAlGaAs, such InGaAs having mole fractions of Al, In, and Ga of the lattice match layer gradually changing with height with a bottom portion having a lattice constant matching GaAs and a top portion having a lattice constant of the InAlAs barrier and InGaAs channel layers;

an InAlAs barrier layer disposed over the lattice match layer;

an $In_y Ga_{1-y} As$ lower channel layer disposed on the barrier layer, where y is the mole fraction of In content in the lower channel layer;

an $In_x Ga_{1-x} As$ upper channel layer disposed on the lower channel layer, where x is the mole fraction of In content in the upper channel layer and where x is different from y;

an InAlAs Schottky layer disposed on the $In_x Ga_{1-x} As$ upper channel layer, and

an InGaAs cap disposed over the InAlAs Schottky layer.

12. The transistor structure recited in claim 11 wherein the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

13. The transistor structure recited in claim 11 wherein the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

14. The transistor structure recited in claim 11 wherein x is in the range between 0.15 and 0.90 and y is in the range between 00.0 and 0.65.

15. The transistor structure recited in claim 14 wherein x is substantially 0.53 and y is substantially 0.43.

16. A transistor structure, comprising:

a semiconductor substrate;

a lattice match layer disposed over the substrate;

an barrier layer disposed over the lattice match layer;

a lower channel layer disposed on the barrier layer;

an upper channel layer disposed on the lower channel layer, such lower channel being of the same material as the upper channel, the upper and lower channels having different mole fractions of an common element used in such upper and lower channel layers; and

an Schottky layer on the upper channel layer.

17. The transistor structure recited in claim 16 wherein the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

18. The transistor structure recited in claim 16 wherein the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

19. The transistor structure recited in claim 17 wherein the substrate comprises GaAs and wherein the upper and lower channel layers comprise InGaAs.

20. The transistor structure recited in claim 19 wherein the upper and lower channel layers include indium.

21. A transistor structure, comprising:

a semiconductor substrate;

an indium aluminum arsenide (InAlGa) barrier layer disposed over the substrate;

an $In_y Ga_{1-y} As$ lower channel layer disposed on the barrier layer, where y is the mole fraction of In content in the lower channel layer;

an $In_x Ga_{1-x} As$ upper channel layer disposed on the lower channel layer, where x is the mole fraction of In content in the upper channel layer and where x is different from y; and an InAlAs Schottky layer on the $In_x Ga_{1-x} As$ upper channel layer.

22. The transistor structure recited in claim 21 wherein the lower channel layer has a bandgap greater that the bandgap of the upper channel layer.

23. The transistor structure recited in claim 22 wherein the lower channel layer has a bulk electron mobility lower than the bulk electron mobility of the upper channel layer.

24. The transistor structure recited in claim 23 wherein x is in the range between 0.15 and 0.90 and y is in the range between 0.0 and 0.65.